BTL2752x

Dual-Channel Low Side Driver

1.Features

- Low side gate driver with two independent output channels
- 5A peak source and sink drive current
- Certain versions with independent enable fucntion for each output
- Fast rise and fall times
- TTL and CMOS compatible logic threshold independent of supply voltage
- Fast Propagation delay (13ns typical)
- Supply undervoltage lockout (UVLO)
- Inputs withstand -5V continuous voltage
- Inputs features Schmitt-trigger characteristic to enhance interference immunity
- Two outputs can be connected in parallel to increase drive current
- Operating temperature -40~140° C
- SOP-8 Option

2.Applications

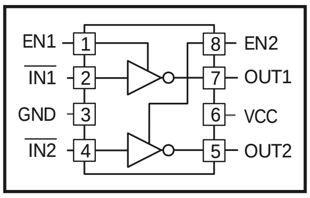
- Solar inverters
- Motor drives
- EV charger
- Industrial power supplies

3.Description

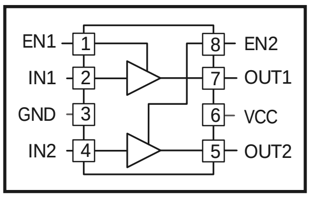
The BTL2752x family of devices are dual-channel, high-speed, low-side gate-drivers, which can deliver high peak current pulses of up to 5A source and 5A sink into capacitive loads along with rail-to-rail drive capability. This also enables connecting two channels in parallel to effectively increase current-drive capability or driving two switches in parallel with one input signal. Dual inverting and dual non-inverting input options are provided.

RoHS
COMPLIANT

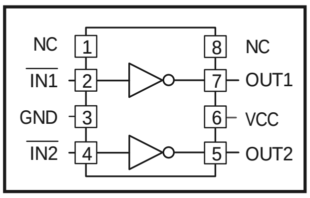
4.Functional Block Diagram



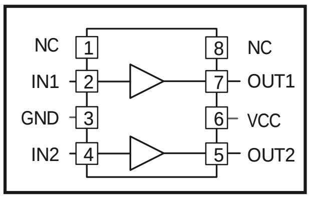
BTL27523



BTL27524



BTL27523B



BTL27524B

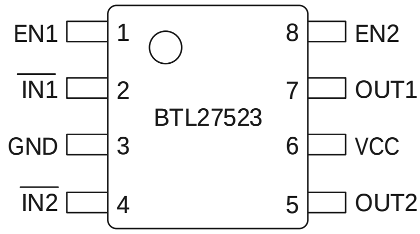
INDEX

5.Product Information

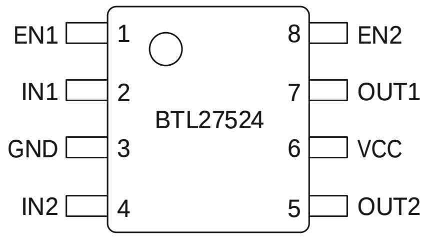
Part No.	Input/Output	Enable Function	Operating	Package	Package Material	MSL Level	Quantity	Device
BTL27523R	Inverting	Yes	-40°C ~140°C	SOP-8	Tape & Reel	MSL1	2500pcs	BTL27523
BTL27523BR		No						BTL27523B
BTL27524R	Non-Inverting	Yes						BTL27524
BTL27524BR		No						BTL27524B

6.Pin Designation

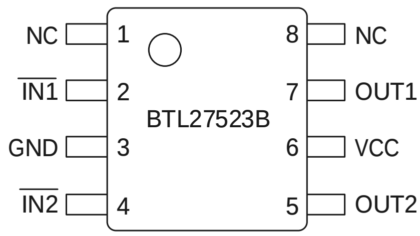
6.1 BTL27523

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	EN1	I	Enable Input for Channel 1	
2	$\overline{\text{IN1}}$	I	Inverting Input to Channel 1	
3	GND	G	Ground	
4	$\overline{\text{IN2}}$	I	Inverting Input to Channel 2	
5	OUT2	O	Output of Channel 2	
6	VCC	P	Power Supply Input	
7	OUT1	O	Output of Channel 1	
8	EN2	I	Enable Input for Channel 2	
(1) P=Power, G=Ground, I=Input, O=Output				

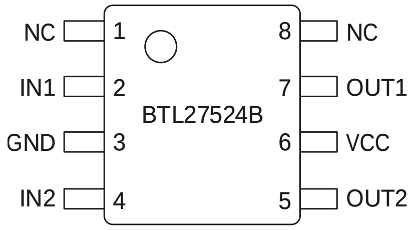
6.2 BTL27524

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	EN1	I	Enable Input for Channel 1	
2	IN1	I	Inverting Input to Channel 1	
3	GND	G	Ground	
4	IN2	I	Inverting Input to Channel 2	
5	OUT2	O	Output of Channel 2	
6	VCC	P	Power Supply Input	
7	OUT1	O	Output of Channel 1	
8	EN2	I	Enable Input for Channel 2	
(1) P=Power, G=Ground, I=Input, O=Output				

6.3 BTL27523B

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	NC	-	No Connected	
2	$\overline{\text{IN1}}$	I	Inverting Input to Channel 1	
3	GND	G	Ground	
4	$\overline{\text{IN2}}$	I	Inverting Input to Channel 2	
5	OUT2	O	Output of Channel 2	
6	VCC	P	Power Supply Input	
7	OUT1	O	Output of Channel 1	
8	NC	-	No Connected	
(1) P=Power, G=Ground, I=Input, O=Output				

6.4 BTL27524B

NO.	NAME	TYPE (1)	DESCRIPTION	PACKAGE
1	NC	-	No Connected	
2	IN1	I	Signal Input to Channel 1	
3	GND	G	Ground	
4	IN2	I	Signal Input to to Channel 2	
5	OUT2	O	Output of Channel 2	
6	VCC	P	Power Supply Input	
7	OUT1	O	Output of Channel 1	
8	NC	-	No Connected	
(1) P=Power, G=Ground, I=Input, O=Output				

7.Specification Parameters

7.1 Absolute Limits

SYMBOL	PARAMETER	MIN	MAX	UNIT
VCC	Supply Voltage range	-0.3 to	24	V
V_O	Output Voltage	-0.3 to	VCC+0.3	
I_{OUT_DC}	Output continuous source/sink current	-	0.3	A
I_{OUT_PEAK}	Output pulsed source/sink current	-	5	
V_{IN}	Input Voltage Range IN, EN	-5	VCC	V
T_J	Operating virtual junction temperature	-40	150	° C
T_S	Storage Temperature	-55	150	
T_L	Soldering Temperature (<10s)	-	300	
ESD	HBM	±4000		V
	CDM	±1000		

Note: 1) These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions.Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability, and cause permanent damage to the device under severe conditions.
2) Unless otherwise specified, all voltages are with respect to GND .Currents are positive into, negative out of the specified terminal.
3) Values are verified by characterization on bench.
4) These devices are electrostatic- sensitive , please comply with the proper device handling procedures.

7.2 Thermal Resistance Information

SYMBOL	PARAMETER	SOP-8	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.0	°C /W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	71.0	
ψ_{JT}	Junction-to-top characterization parameter	37.4	
ψ_{JB}	Junction-to-board characterization parameter	81.4	

7.3 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNIT
VCC	Input supply voltage	4.5	20	V
V_{IN}	Input Voltage IN, EN	0	VCC	
T_A	Operating temperature	-40	140	°C

7.4 Electrical Characteristics

T_A=-40~140°C , VCC=12V.Output pin: current towards outside of the chip is positive direction; Input pin: current towards inside of the chip is positive direction.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(off)}$	Starting current (based on Input configuration)	VCC=3.3V, IN1=IN2=VCC/IN1=IN2=GND	25	40	80	μA
V_{IH}	Input logic 0 → 1 (IN1, IN2, EN)	-	1.80	2.00	2.30	V
V_{IL}	Input logic 1 → 0 (IN1, IN2, EN)	-	0.95	1.15	1.35	
V_{IN-HYS}	Input hysteresis	-	0.70	0.85	1.00	
V_{ON}	Supply start threshold	-	3.6	4	4.4	
V_{OFF}	Minimum operating voltage after supply start	-	3.3	3.7	4.1	
V_{UV-HYS}	Undervoltage hysteresis	-	-	0.3	-	
I_{OUT}	Sink/source peak current	C_L=220nF, f_{SW}=1kHz	-	+5	-	A
I_{VTS}	OUTx pin sink current	2μs	-	-5	-	
VCC-V_O	High output voltage	I_{OUT}=10mA	-	-	75	mV
V_O-GND	Low output voltage	I_{OUT}=-10mA	-	-	15	
R_{ON}	Output pullup resistance	I_{OUT}=10mA	2.5	3.5	5.5	Ω
R_{OFF}	Output pulldown resistance	I_{OUT}=-10mA	0.5	1	1.5	
R_{EN}	EN pin internal pull-up resistor	-	-	200	-	kΩ
R_{IN}	Input pull-up resistance (BTL27523)	-	-	200	-	
	Input pull-down resistance (BTL27524)	-	-	400	-	
t_{on}	Turn-on Propagation delay	C_L=1.8nF, f_{SW}=1kHz	6	13	23	ns
t_{off}	Turn-off propagation delay	C_L=1.8nF, f_{SW}=1kHz	6	13	23	
t_r	Rise time	C_L=1.8nF	-	16	18	
t_f	Fall time	C_L=1.8nF	-	15	18	
t_M	Propagation delay matching between 2 channels	IN1=IN2	-	-	4	
t_{PW}	Minimum input pulse width that changes the output state	-	-	15	40	
t_{UVLO}	UVLO recovery time	-	-	50	-	μs

8.Parameter Testing

8.1 Typical Characteristics

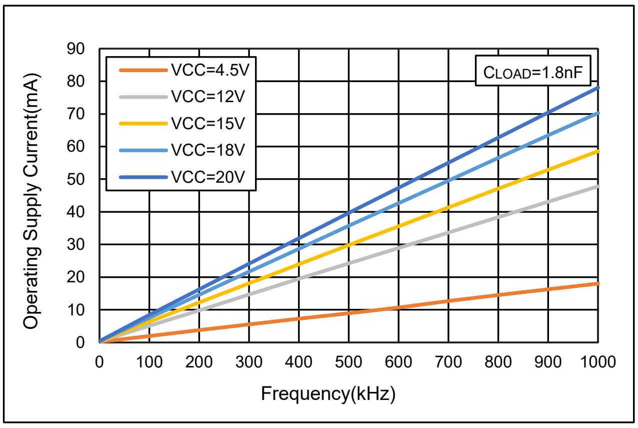


Figure 1. Operating Supply Current vs Frequency

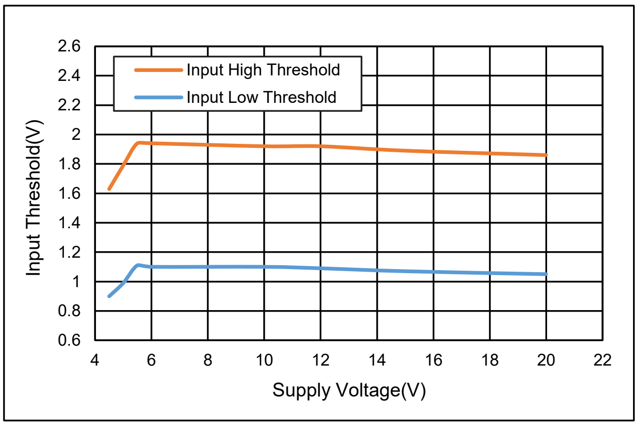


Figure 2. Input Threshold vs Supply Voltage

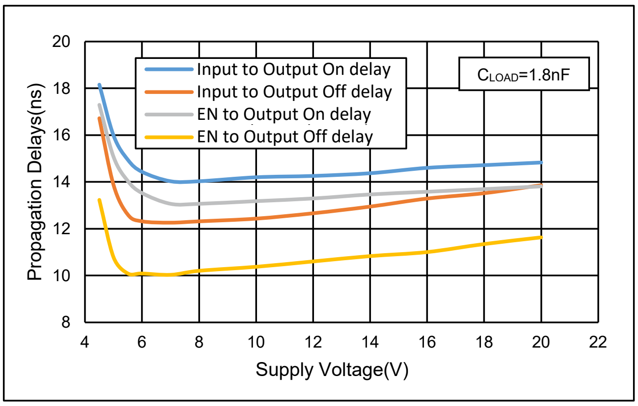


Figure 3. Propagation Delay vs Supply Voltage

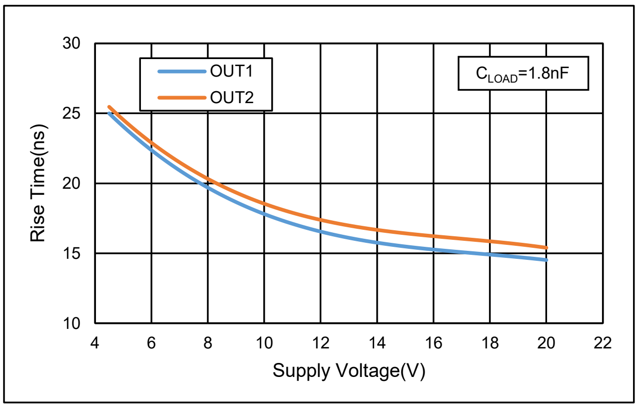


Figure 4. Rise Time vs Supply Voltage

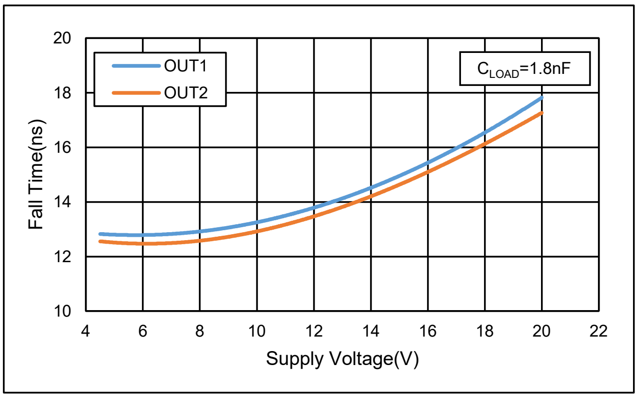


Figure 3. Fall Time vs Supply Voltage

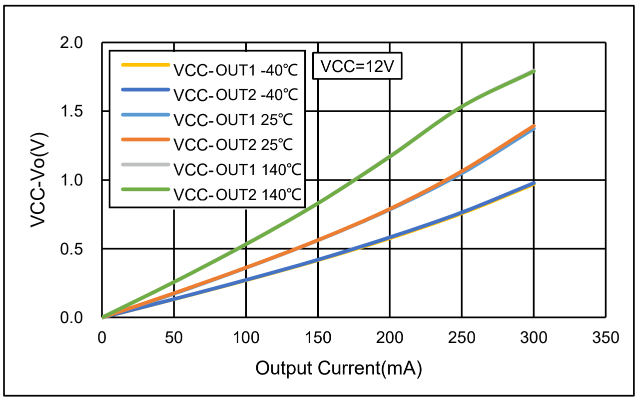


Figure 6. VCC-Vo vs Output Current

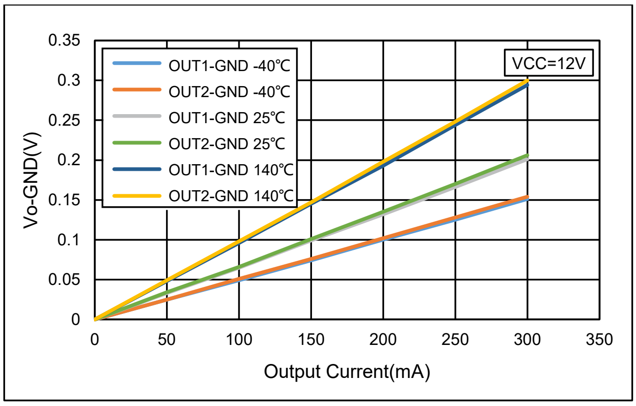


Figure 7. Vo-GND vs Output Current

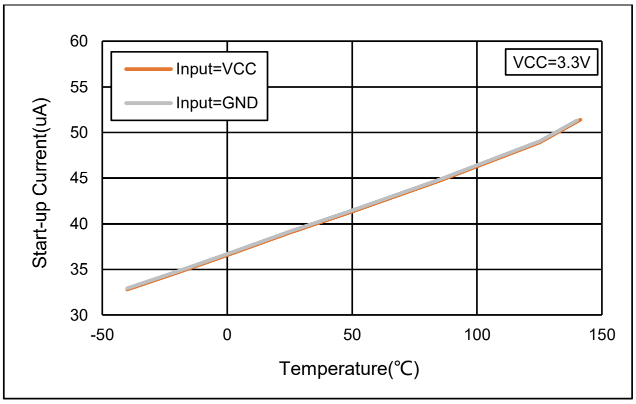


Figure 8. Start-Up Current vs Temperature

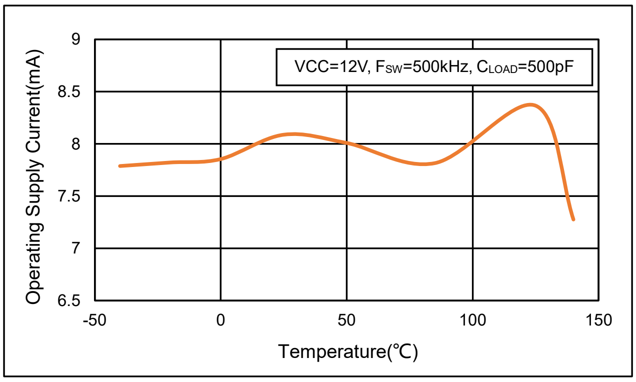


Figure 9. Operating Supply Current vs Temperature

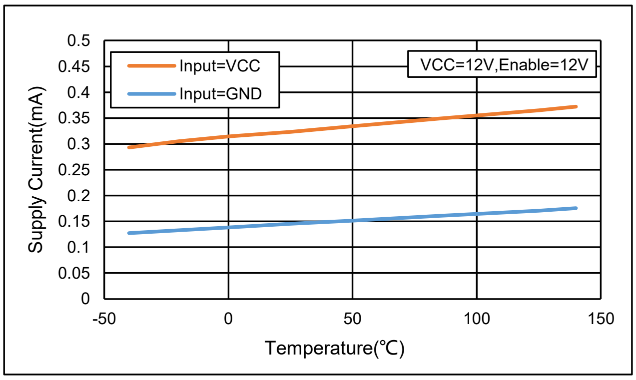


Figure 10. Supply Current vs Temperature (Outputs in DC ON/OFF Condition)

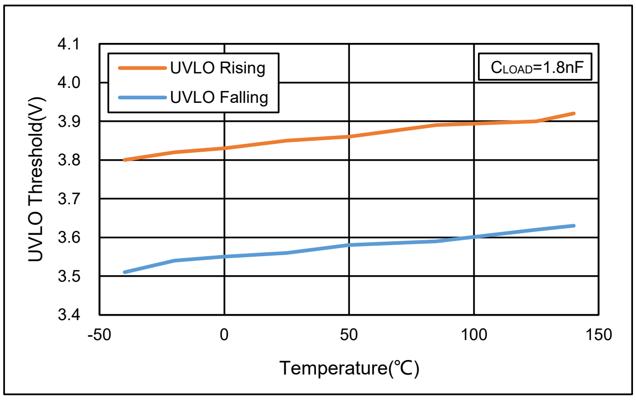


Figure 11. UVLO Threshold vs Temperature

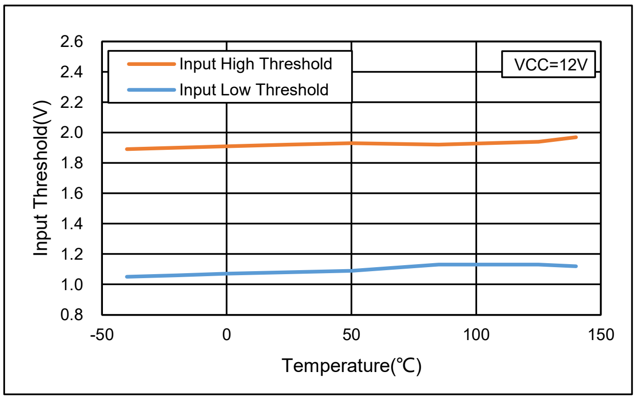


Figure 12. Input Threshold vs Temperature

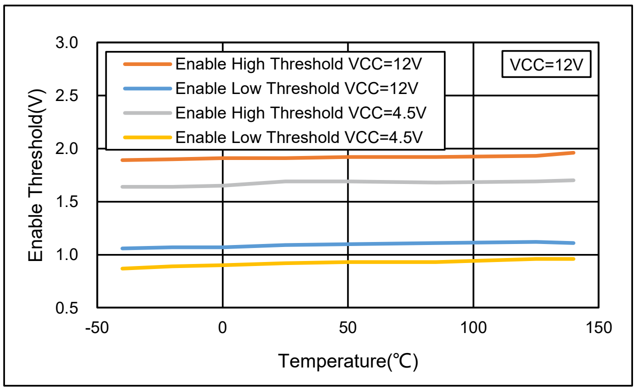


Figure 13. Enable Threshold vs Temperature

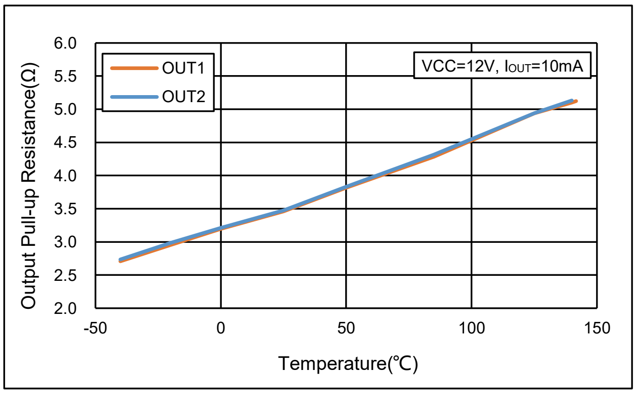


Figure 14. Output Pull-up Resistance vs Temperature

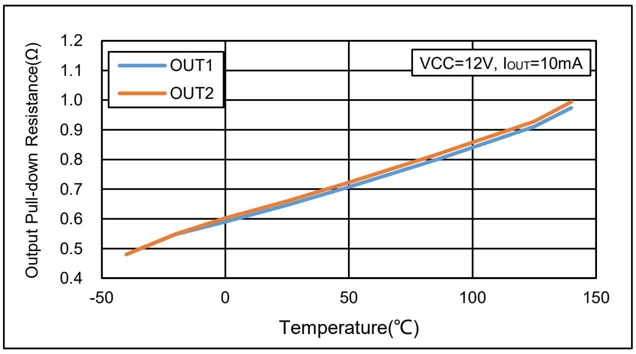


Figure 15. Output Pull-down Resistance vs Temperature

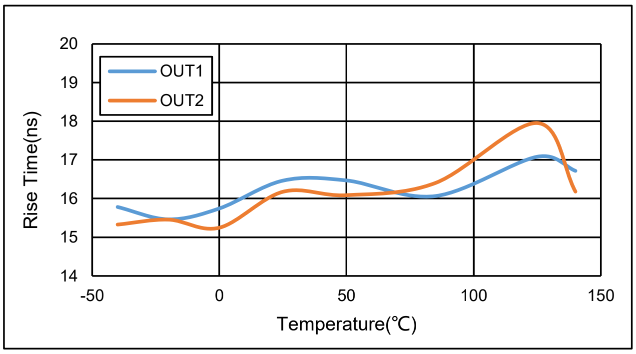


Figure 16. Rise Time vs Temperature

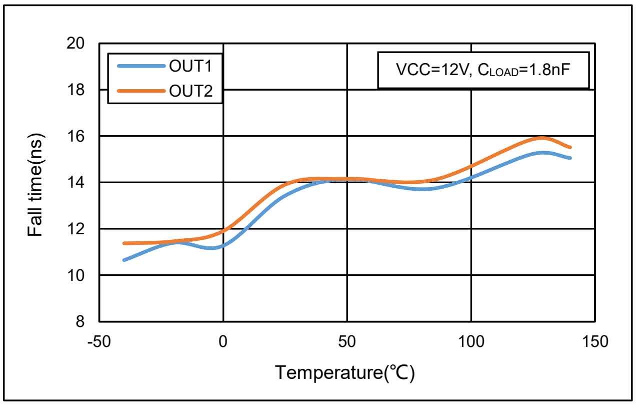


Figure 17. Fall Time vs Temperature

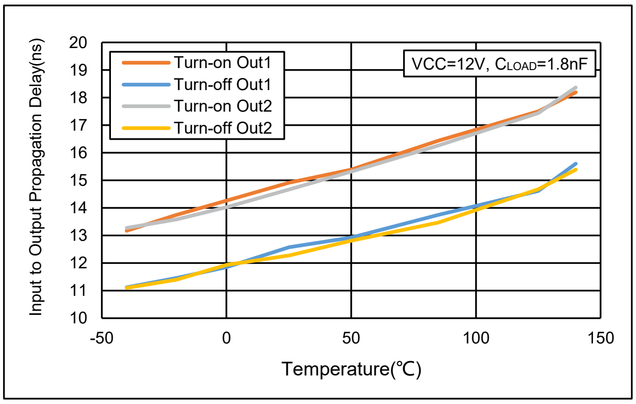


Figure 18. Input to Output Propagation Delay vs Temperature

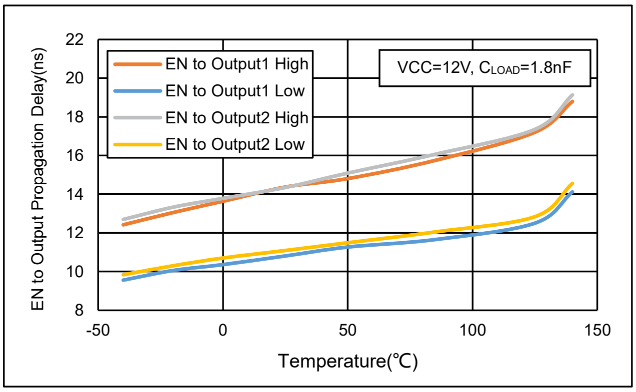


Figure 19. EN to Output Propagation Delay vs Temperature

8.2 Propagation Delay

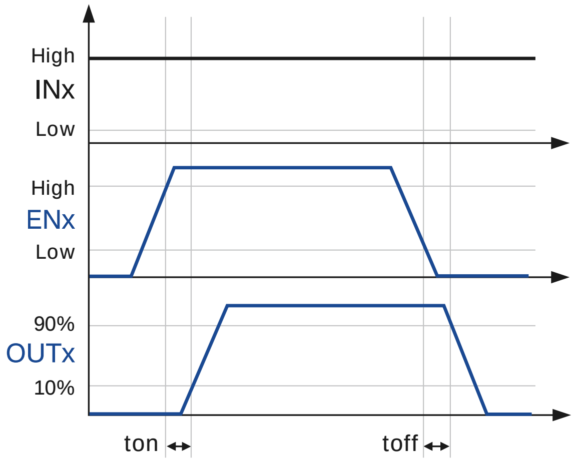


Figure 20. BTL27524 Enable Function

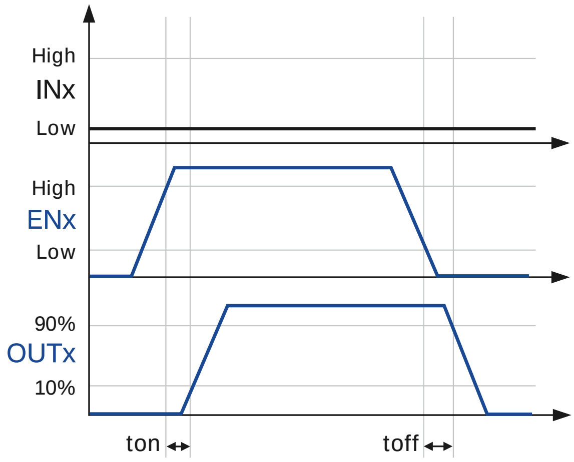


Figure 21. BTL27523 Enable Function

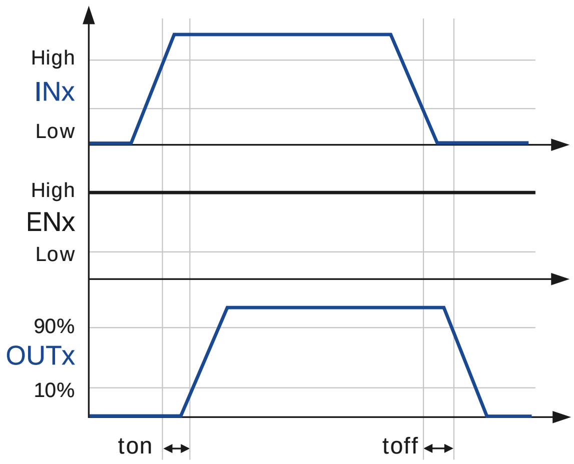


Figure 22. Non-inverting input driver operation (BTL27524)

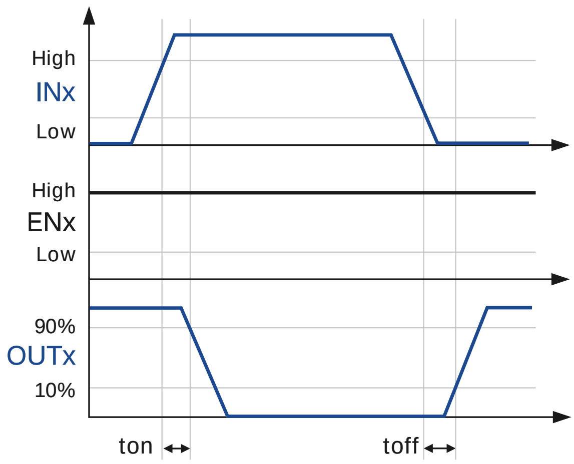


Figure 23. Inverting input driver operation (BTL27523)

9.Function Description

9.1 Input Stage

BTL2752x's input pins are based on a TTL and CMOS compatible input-threshold logic, and support 3.3V, 5V and 15V, so that the chip can be driven by multiple logic levels. The input pins are equipped with Schmitt stage internally to enhance noise immunity. BTL27524's input pins contain 400kΩ pulldown resistor to GND, and BTL27523's input pins contain 200kΩ VCC pullup resistor, ensuring that the output of the device is low when the inputs are left open. However, in order to secure the initial power-on state of the driver IC, it is recommended to add appropriate extra pull-up or pull-down resistors to the input.

9.2 Enable

BTL2752x devices are provided with independent enable pins ENx for enabling of each driver channel. When the ENx pins are high, the driver is enabled. When the ENx pins are low, the driver is disabled. Like the input pins, the enable pins are also compatible with TTL and CMOS logic levels, support 3.3V, 5V and 15V. The enable pins are equipped with Schmitt stage internally to enhance noise immunity. The ENx pins are internally pulled up to VCC by a 200kΩ resistor, therefore the outputs of the device are enabled if the ENx pins are left open.

9.3 Output Stage

The BTL2752x has a rail-to-rail push stage output. The output stage pullup structure includes a P-channel MOSFET and an N-channel MOSFET in parallel. The P-channel MOSFET provides a low conduction voltage drop during static conduction (Figure 24). The pull-down structure is implemented using an N-channel MOSFET. An 1MΩ resistor is connected in parallel between the drain and gate of the MOSFET to effectively clamp the gate voltage of the power device in the event of power down to prevent the occurrence of partial turn-on. However, in order to ensure reliable shutdown of the power device, it is recommended to add extra pull-down resistor to the gate.

9.4 Undervoltage Lockout

The BTL2752x has undervoltage lockout (UVLO) protection function on the power supply VCC pin to prevent the gate drive voltage from being insufficient. When the supply voltage is below UVLO threshold, the AISC turns off the output to protect the power devices. When the supply voltage reaches the clear fault threshold, the AISC resumes the output. To prevent repeated action near the UVLO threshold, hysteresis is applied. In order to avoid the uncertainty of the output state after power-on, the AISC firstly enters an UVLO state after power-on, turns off the output until the supply voltage is established and then starts normal operation (Figure 25).

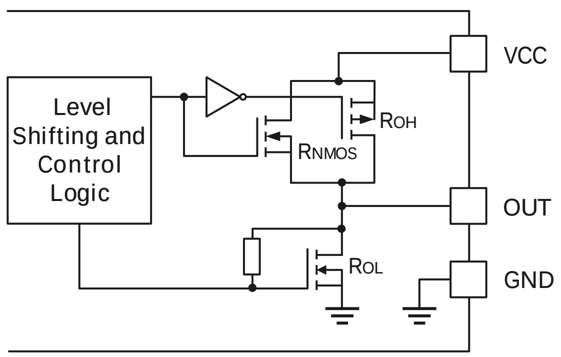


Figure 24. Output Structure

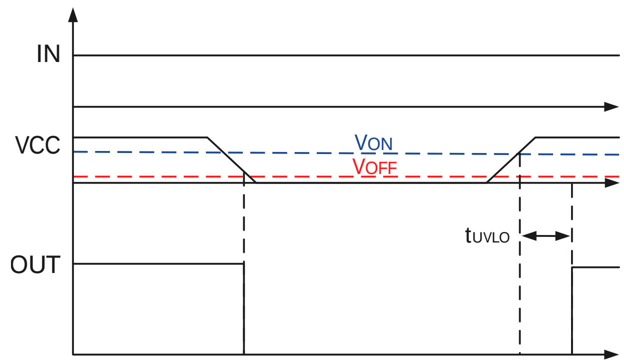


Figure 25. Undervoltage Lockout

9.5 Device Logic Table

BTL27523 and BTL27524

EN	IN	OUT	
		BTL27523	BTL27524
H	H	L	H
H	L	H	L
Floating	H	L	H
Floating	L	H	L
Any	Floating	L	L
L	Any	L	L

BTL27523B and BTL27524B

IN	OUT	
	BTL27523B	BTL27524B
H	L	H
L	H	L
Floating	L	L

10.Applications

This sections introduces the typical application of Bronze Technologies driver ICs, which is for reference only. In practical application, users need to verify and test its applicability according to their own design requirements to confirm the system function.

10.1 Typical Applications

Bronze Technologies recommends that customers add a RC filter with a small time constant at the input port to filter out high-frequency interference, without adding up significant delay.It is recommended that the resistance value should be between 0 and 100Ω and the capacitance should be less than 1000pF.When setting this parameter, the influence between high frequency interference and delay needs to be taken into account. To ensure the supply stability, Bronze Technologies recommends adding appropriate blocking capacitors between the supply pin and GND. It is recommended to connect 1uF+0.1uF capacitor bewteen VCC-GND pins. The two channels of BTL2752x can be connected in parallel to achieve a higher driving current.

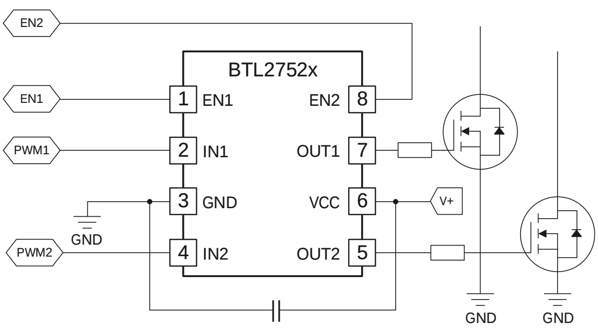


Figure 26. BTL2752x Typical Application Diagram

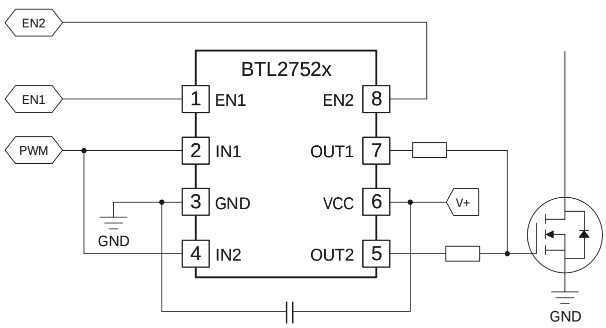
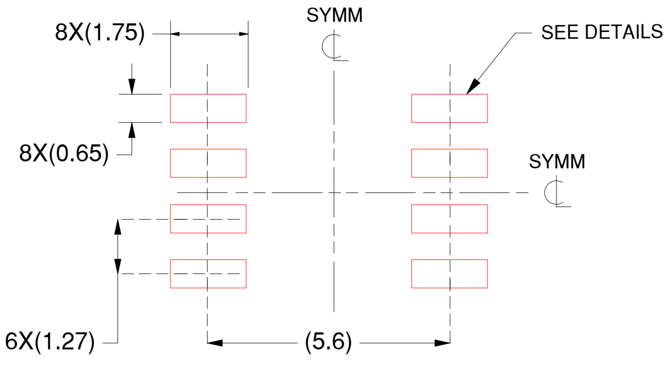


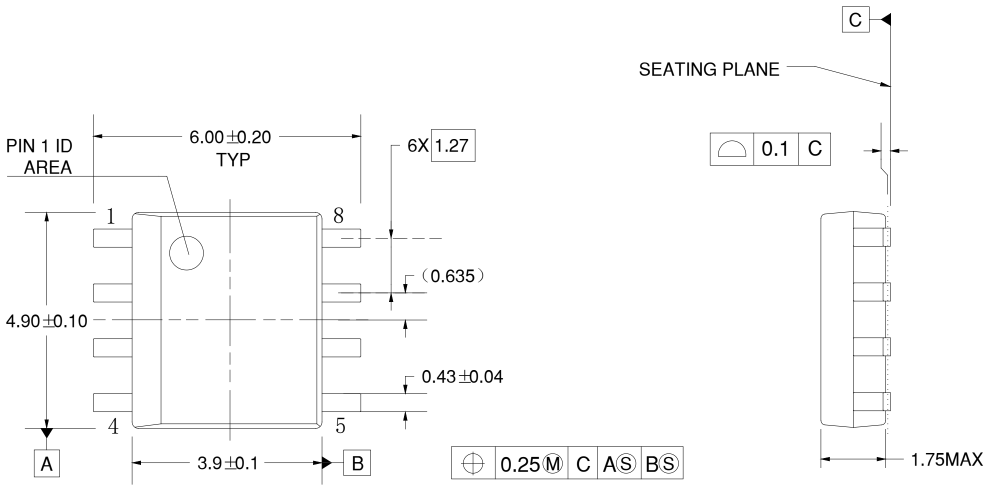
Figure 27. BTL2752x Application Diagram with Two Outputs Connected in Parallel

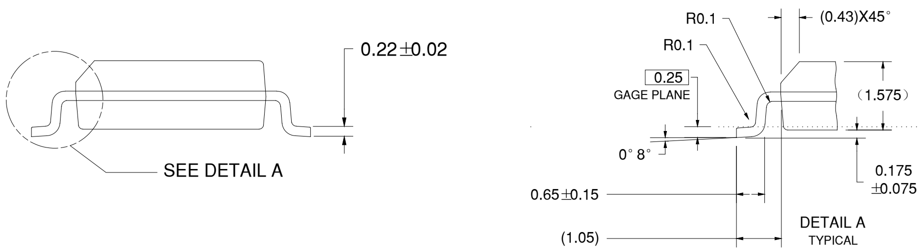
11.Package Information

11.1 SOP-8 Package



SOLDER PASTE EXAMPLE



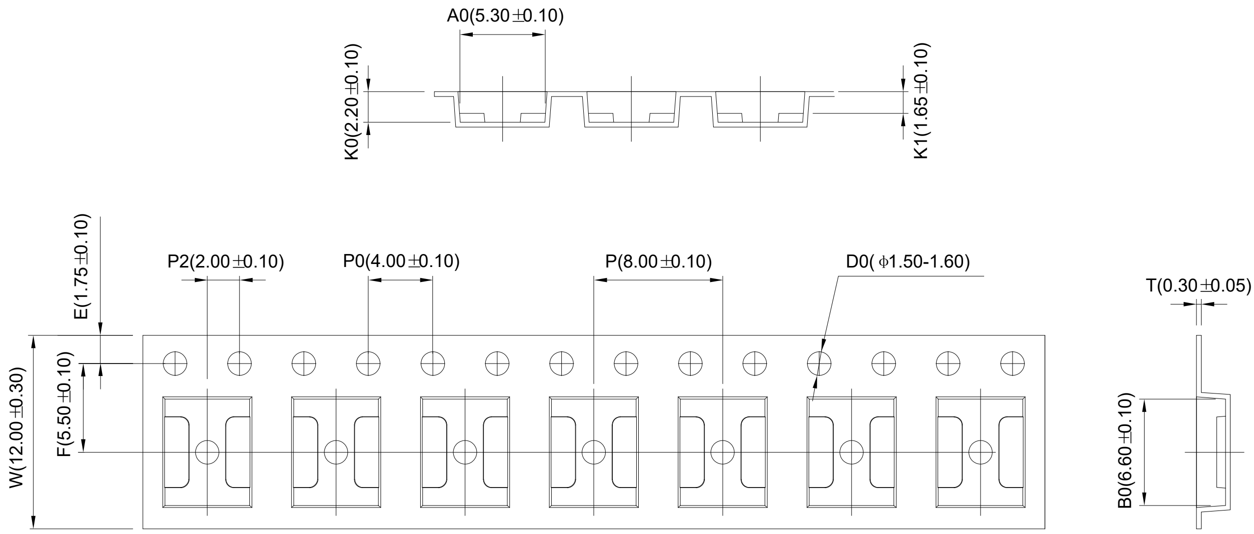


Note: 1)Legend unit: mm.

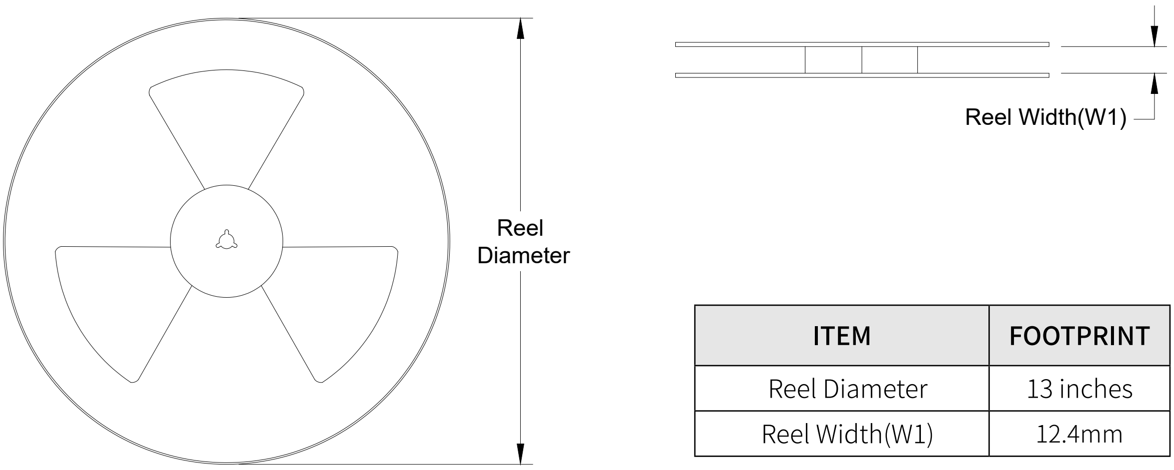
Electrostatic Discharge Caution

If proper handling and installation procedures are not followed, the ICs may be damaged.ESD damage can cause minor degradation of performance and severe failure of the entire device. Precision integrated circuits may be more susceptible to damage because very small parameter changes may cause the device to fail to meet its published specifications.

11.2 Packing Information



REEL DIMENSIONS



ITEM	FOOTPRINT
Reel Diameter	13 inches
Reel Width(W1)	12.4mm

12.Version Description

REVISION	NOTES	DATE
Rev.0.0	Released datasheet	07-Jan-2023
Rev.0.1	Changed source/sink drive current from 4A to 5A, added input withstand voltage of -5V	14-Mar-2023
Rev.0.2	added Typical Characteristics	08-Mar-2024

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